

CLAIMS

We claim:

1. A signal processing apparatus, comprising:
  - a time-interleaved system operable to distribute a signal into a first processing pathway and, following a predetermined amount of time, into a second processing pathway; and
    - a delay structure coupled to said second processing pathway, said delay structure including at least one floating-gate field effect transistor,
      - wherein the predetermined amount of time depends on an amount of electrical charge stored on the floating gate of the at least one floating-gate field effect transistor.
2. The signal processing apparatus of claim 1 wherein the signal processing apparatus comprises an analog-to-digital converter.
3. The signal processing apparatus of claim 1 wherein the signal processing apparatus comprises a quadrature mixing circuit.
4. A signal processing apparatus, comprising:
  - an input node configured to receive a signal;
  - a splitter operable to split the signal into a first signal portion and a second signal portion and direct the first signal portion to a first node and directing the second signal portion to a second node; and

a first circuit coupled between said first node and a third node, said first circuit including a first analog-valued floating-gate transistor operable to effect a time delay on the first signal portion depending on an amount of electrical charge stored on a floating gate of said first transistor.

5. The signal processing apparatus of claim 4, further comprising a second circuit coupled between said second node and a fourth node.

6. The signal processing apparatus of claim 5, further comprising a combiner operable to combine signals from outputs of said first and second circuits.

7. The signal processing apparatus of claim 6 wherein said second circuit includes a second analog-valued floating-gate transistor operable to effect a time delay on the second signal portion depending on an amount of electrical charge stored on a floating gate of said second transistor.

8. A signal processing apparatus, comprising:  
a signal processing path including two or more signal processing elements; and  
a time delay element disposed between adjacent processing elements of the two or more signal processing elements, said time delay element including at least one analog-valued floating-gate field effect transistor,

wherein a time delay of said time delay element depends on an amount of electrical charge stored on the floating gate of the at least one analog-valued floating-gate field effect transistor.

9. The signal processing apparatus of claim 8, further comprising a combiner configured to receive and combine output signals from said adjacent processing elements.

10. An apparatus for processing a signal, comprising:

- an input node configured to receive a signal;
- an intermediate node;
- an output node;
- a first circuit coupled between said input node and said intermediate node, said first circuit including a first analog-valued floating-gate transistor operable to effect a time delay on the signal received at said input node depending on an amount of electrical charge stored on a floating gate of said first transistor; and
- a second circuit disposed between said intermediate node and said output node.

11. The apparatus of claim 10 wherein said second circuit includes a second analog-valued floating-gate transistor operable to effect a time delay on an intermediate signal received at said intermediate node depending on an amount of electrical charge stored on a floating gate of said second transistor.

12. An apparatus for processing a signal, comprising:

an input node configured to receive an input signal;

a splitter operable to split the input signal into at least a first signal portion and a second signal portion and direct the first signal portion to a first node and direct the second signal portion to a second node;

a first circuit coupled between said first node and a third node, said first circuit including a first analog-valued floating-gate transistor operable to effect a time delay on the first signal portion depending on an amount of electrical charge stored on a floating gate of said first transistor; and

a second circuit coupled between said second node and a fourth node, said second circuit including a first analog-valued floating-gate transistor operable to effect a time delay on the second signal portion received depending on an amount of electrical charge stored on a floating gate of said second transistor.

13. A method of processing a signal, comprising:

receiving an input signal at an input node;

splitting said input signal into a first portion and a second portion;

processing said first portion using a first circuit comprising a first analog-valued floating-gate transistor, said step of processing said first portion including effecting a time delay on said first portion depending on an amount of electrical charge stored on a floating gate of said first transistor; and

processing said second portion.

14. The method of claim 13, further comprising a step of combining the processed first and second portions.

15. The method of claim 13 wherein the step of processing said second portion includes using a second circuit comprising a second analog-valued floating-gate transistor, said second step of processing said second portion including effecting a time delay on said second portion depending on an amount of electrical charge stored on a floating gate of said second transistor.

16. A method of processing a signal, comprising:  
processing an input signal into an intermediate signal using a first circuit comprising a first analog-valued floating-gate transistor, said step of processing said input signal including effecting a time delay on said input signal depending an amount of electrical charge stored on a floating gate of said first transistor; and  
processing said intermediate signal into an output signal.

17. The method of claim 16 wherein said step of processing said intermediate signal includes using a second circuit comprising a second analog-valued floating-gate transistor, said step of processing said intermediate signal including effecting a time delay on said intermediate signal depending on an amount of electrical charge stored on a floating gate of said second transistor.

18. A delay element for effecting a delay in a signal path of an electric circuit, said delay element comprising an analog-valued floating-gate transistor.

19. The delay element of claim 18, further comprising a CMOS inverter including a PMOS transistor with a source that is coupled to a drain of the analog-valued floating-gate transistor.

20. An apparatus comprising at least one analog-valued floating-gate transistor, wherein an operating characteristic of the apparatus depends on an amount of electrical charge stored on a floating gate of said at least one analog-valued floating-gate transistor.

21. The apparatus of claim 20 wherein the operating characteristic is a delay effected on a signal operated on by the apparatus.

22. The apparatus of claim 20 wherein the apparatus is a time-interleaved system.

23. The apparatus of claim 20 wherein the apparatus is a pipelined system.

24. The apparatus of claim 21 wherein the apparatus is a time-interleaved system.

25. The apparatus of claim 21 wherein the apparatus is a pipelined system.
26. An apparatus according to claim 20 wherein the apparatus is a digital-to-analog converter, an analog-to-digital converter, a track-and-hold circuit, a finite impulse response filter, a mixer, an RC filter, or an amplifier.
27. A signal processing apparatus, comprising:
  - means for receiving an input signal at an input node;
  - means for splitting said input signal into a first portion and a second portion;
  - means for processing said first portion using a first circuit comprising a first analog-valued floating-gate transistor, said means for processing said first portion including effecting a time delay on said first portion depending on an amount of electrical charge stored on a floating gate of said first transistor; and
  - means for processing said second portion.
28. The signal processing apparatus of claim 27, further comprising means for combining the processed first and second portions.
29. The signal processing apparatus of claim 27 wherein the means for processing said second portion includes using a second circuit comprising a second analog-valued floating-gate transistor, said means for processing said second portion

including affecting a time delay on said second portion depending on an amount of electrical charge stored on a floating gate of said second transistor.

30. A signal processing apparatus, comprising:

means for processing an input signal into an intermediate signal using a first circuit comprising a first analog-valued floating-gate transistor, said means for processing said input signal including effecting a time delay on said input signal depending an amount of electrical charge stored on a floating gate of said first transistor; and

means for processing said intermediate signal into an output signal.

31. The signal processing apparatus of claim 30 wherein said means for processing said intermediate signal includes using a second circuit comprising a second analog-valued floating-gate transistor, said means for processing said intermediate signal including effecting a time delay on said intermediate signal depending on an amount of electrical charge stored on a floating gate of said second transistor.

32. A signal processing apparatus, comprising:

a time-interleaved system having two or more signal processing pathways, each signal processing pathway configured to receive a common input signal; and

one or more delay structures disposed in one or more of said two or more signal processing pathways, each delay structure including at least one floating-gate field effect transistor.

33. A signal processing apparatus, comprising:
  - an electrical circuit; and
  - a floating-gate field effect transistor disposed in a first circuit pathway of the circuit,
    - wherein an amount of charge present on the floating gate of the floating-gate transistor is used to match a first circuit characteristic in the first circuit pathway to a second circuit characteristic in a second circuit pathway of the circuit.
34. The signal processing apparatus of claim 33 wherein the first and second circuit characteristics correspond to relative delays presented to signals transmitted in the first and second circuit pathways.
35. The signal processing apparatus of claim 33 wherein the first and second circuit characteristics correspond to relative gains of circuit elements in the first and second circuit pathways.
36. The signal processing apparatus of claim 33 wherein the first and second circuit characteristics relate to clock timing, frequency response, offset or transfer functions of the first and second circuit pathways.
37. The signal processing apparatus of claim 33 wherein the circuit comprises a pipelined circuit.

38. The signal processing apparatus of claim 33 wherein the circuit comprises a time-interleaved circuit.

39. The signal processing apparatus of claim 33 wherein the circuit comprises an analog-to-digital converter.

40. The signal processing apparatus of claim 34 wherein the circuit comprises an analog-to-digital converter.

41. The signal processing apparatus of claim 35 wherein the circuit comprises an analog-to-digital converter.

42. The signal processing apparatus of claim 33 wherein the circuit comprises a digital-to-analog converter.

43. The signal processing apparatus of claim 35 wherein the circuit comprises a digital-to-analog converter.

44. The signal processing apparatus of claim 33 wherein the charge stored on the floating gate can be modified during operation of the circuit.

45. A signal processing apparatus, comprising:

means for receiving an input signal at an input node of a circuit;  
means for splitting the input signal into first and second circuit paths of said circuit;  
a floating-gate field effect transistor disposed in the first circuit path; and  
means for modifying a first circuit characteristic in the first circuit path relative to a second circuit characteristic in the second circuit path by adjusting an amount of charge stored on a floating of the floating-gate field effect transistor.

46. The signal processing apparatus of claim 45 wherein the first circuit characteristic comprises a delay presented to a signal transmitted in the first circuit path.

47. The signal processing apparatus of claim 45 wherein the first circuit characteristic comprises a gain of a circuit element disposed in the first circuit path.

48. The signal processing apparatus of claim 45 wherein the first circuit characteristic relates to clock timing, frequency response, offset or transfer function of the first circuit path.

49. The signal processing apparatus of claim 45 wherein the circuit comprises a pipelined circuit.

50. The signal processing apparatus of claim 45 wherein the circuit comprises a time-interleaved circuit.

51. The signal processing apparatus of claim 45 wherein the means for modifying is operational during times when the signal processing apparatus is operating.